In The Claims:

95. (Currently amended) A process for fabricating a state change element in a 3-D semiconductor memory device comprising the steps of:

(a) forming a semiconductor layer; ~~and~~

(b) oxidizing at least a portion of the semiconductor layer in a plasma to form an oxide antifuse layer overlying the semiconductor layer; and

(c) repeating steps a and b for multiple memory layers, each memory layer comprising vertically fabricated memory cells.

96. (Previously added) The process of claim 95, wherein the step of oxidizing at least a portion of the semiconductor layer comprises oxidizing at a temperature of no more than about 400°C.

97. (Previously added) The process of claim 95, wherein the step of oxidizing at least a portion of the semiconductor layer comprises a self-limiting oxidation process having an oxidation rate, and wherein the oxidation rate gradually decreases during the oxidation process.

98. (Previously added) The process of claim 95, wherein the step of forming a semiconductor layer comprises forming a layer of polycrystalline silicon doped with a conductivity determining dopant.

99. (Previously added) The process of claim 95, wherein the step of forming a semiconductor layer comprises forming a layer of amorphous silicon.

100. (Previously added) The process of claim 95, wherein the step of forming a semiconductor layer comprises forming a layer of recrystallized silicon.

101. (Withdrawn) A process for fabricating a memory cell comprising:
forming a steering element; and
forming a state change element adjacent to the steering element,
wherein the state change element includes a dielectric rupture layer, and
wherein the dielectric rupture layer is formed by a plasma oxidation process.

102. (Withdrawn) The process of claim 101, wherein the plasma oxidation process forms an oxide layer on a semiconductor material within the state change element.

103. (Withdrawn) The process of claim 101, wherein the step of forming a steering element comprises forming a steering element containing metal elements, and wherein the plasma oxidation process is carried out at a temperature below that at which the metal elements can interdiffuse in the steering element.

104. (Withdrawn) The process of claim 103, wherein the plasma oxidation process comprises a process carried out at no more than about 400°C.

105. (Withdrawn) The process of claim 103, wherein the step of forming a steering element containing metal elements comprises forming a refractory metal.

106. (Withdrawn) The process of claim 103, wherein the step of forming a steering element containing metal elements comprises forming a refractory metal silicide.

107. (Currently amended) A process for fabricating a cell in a 3-D semiconductor memory device comprising:

forming a first conductor layer;

forming a first semiconductor layer overlying the conductor layer;

oxidizing at least a portion of the first semiconductor layer in a plasma to form an oxide layer thereon;

forming a second semiconductor layer overlying the oxide layer;

~~forming a second conductor layer overlying the second semiconductor layer; and~~

sequentially etching the second semiconductor layer, the oxide layer, the first semiconductor layer and the first conductor layer to form a line;

forming a second conductor layer overlying the line; and

sequentially etching the second conductor layer and the line to form a pillar of the 3-D semiconductor memory device.

108. (Previously added) The process of claim 107, wherein the step of oxidizing at least a portion of the first semiconductor layer comprises plasma oxidation at a temperature of no more than about 400°C.

109. (Previously added) The process of claim 107, wherein the step of forming a first conductor layer comprises forming a conductor layer including metal elements, and wherein the step of oxidizing at least a portion of the first semiconductor layer comprises a plasma oxidation process carried out at a temperature below that at which the metal elements can interdiffuse in the conductor layer.

110. (Previously added) The process of claim 109, wherein the step of forming a conductor layer containing metal elements comprises forming a refractory metal.

111. (Presently amended) The process of claim 109, wherein the step of forming a ~~steering element~~ conductor layer containing metal elements comprises forming a refractory metal silicide.

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112. (Previously added) The process of claim 107, wherein the step of sequential etching comprises forming edge regions on the pillar, and wherein the process further comprises oxidizing the edge region using a plasma oxidation process.

113. (Previously added) The process of claim 107, wherein the step of forming a first semiconductor layer comprises forming a layer of polycrystalline silicon doped with a conductivity determining dopant.

114. (Previously added) The process of claim 107, wherein the step of forming a first semiconductor layer comprises forming a layer of amorphous silicon.

115. (Previously added) The process of claim 107, wherein the step of forming a first semiconductor layer comprises forming a layer of recrystallized silicon.

116. (New) A process for fabricating a single element antifuse in a 3-D semiconductor memory device comprising:

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forming a first active electrode layer;

oxidizing at least a portion of the first active electrode layer in a plasma to form an oxide antifuse layer thereon; and

forming a second active electrode layer overlying and in intimate contact with oxide antifuse layer.

117. (New) The process of claim 116, wherein the first active electrode layer comprises an anode, and wherein the second active electrode layer comprises a cathode.

118. (New) The process of claim 116, wherein the first active electrode layer comprises a cathode, and wherein the second active electrode layer comprises an anode.

119. (New) The process of claim 116 further comprising forming a first conductor lead below the first active electrode layer and forming a second conductor lead above the second active electrode layer, wherein each of the first and second conductor leads are orthogonally disposed relative to one another.

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120. (New) A process for fabricating a 3-D semiconductor memory device comprising the steps of:

forming a first stack comprising a state change element; and

forming a second stack comprising a state change element overlying the first stack,

wherein forming each of the first stack and the second stack comprises forming a semiconductor layer; and

oxidizing at least a portion of the semiconductor layer in a plasma to form an oxide antifuse layer overlying the semiconductor layer.

121. (New) The process of claim 120 further comprising forming orthogonally disposed conductor leads above and below each of the first and second stacks.

122. (New) A process for fabricating a cell in a 3-D semiconductor memory device comprising:

forming a first conductor layer;

forming a first semiconductor layer overlying the first conductor layer;

oxidizing at least a portion of the first semiconductor layer to form an oxide layer thereon;

forming a second semiconductor layer overlying the oxide layer;

sequentially etching the second semiconductor layer, the oxide layer, the first semiconductor layer, the first conductor layer to form a line;

forming a second conductor layer overlying the first line;

etching the second conductor layer to form a second line orthogonal to the first line and etching the first line to form a pillar; and

forming edge regions on the pillar using a plasma oxidation process.

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123. (New) A process for fabricating a 3-D semiconductor memory device comprising the steps of:

forming a first stack comprising a steering element and a state change element;

forming a second stack comprising a steering element and a state change element overlying the first stack,

wherein the first and second stacks comprise elements of a pillar in a 3-D memory array, and

forming edge regions on the pillar using a plasma oxidation process.

124. (New) The process of claim 122, wherein forming a first stack comprises:

forming a bottom conductor layer;

forming a bottom semiconductor layer overlying the conductor layer;

oxidizing at least a portion of the bottom semiconductor layer in a plasma to form an oxide layer thereon;

forming a top semiconductor layer overlying the oxide layer; and